

Biologically-Inspired Electronics with Memory Circuit Elements

Massimiliano Di Ventra and Yuriy V. Pershin

Abstract Several unique properties of biological systems, such as adaptation to natural environment, or of animals to learn patterns when appropriately trained, are features that are extremely useful, if emulated by electronic circuits, in applications ranging from robotics to solution of complex optimization problems, traffic control, etc. In this chapter, we discuss several examples of biologically-inspired circuits that take advantage of memory circuit elements, namely, electronic elements whose resistive, capacitive or inductive characteristics depend on their past dynamics. We provide several illustrations of what can be accomplished with these elements including learning circuits and related adaptive filters, neuromorphic and cellular computing circuits, analog massively-parallel computation architectures, etc. We also give examples of experimental realizations of memory circuit elements and discuss opportunities and challenges in this new field.

1 Introduction

Reproducing some of the features that are commonly found in living organisms, including - as the ultimate, and most sought after goal - the workings of the human brain, is what "artificial intelligence" is all about [1]. However, even without aiming for such an ambitious target, there are several tasks that living organisms perform seamlessly and, when reproduced in electronic circuits, are of great benefit and help us solve complicated problems. The main idea of *biologically-inspired electronics* is

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thus in borrowing approaches used by biological systems interacting with their environment and in applying them in diverse technological areas requiring, for example, adaptation to changing inputs, analog solution of optimization problems – one of the well-known approaches to this problem is the “ant-search algorithm” [2, 3] –, associative memory and unlearning, binary and fuzzy logic, etc.

If we look closer, it is evident that if we want to reproduce any of these tasks with electronic circuits, two main characteristics have to be satisfied by some of the circuit elements or their combinations. These elements need to *i)* store information – they have to have memory of the past – and *ii)* be dynamical – their states have to vary in time in response to a given input, preferably in a non-linear way. The latter requirement will help building a wide range of electronic circuits of desired functionality.

Circuits based on active elements (such as transistors) can clearly perform both tasks, however, at a high cost of power consumption, low density, and complexity. It would be much more desirable if we could combine the above features in single, passive elements, preferably with dimensions at the nanometer scale, and hence comparable to – or even smaller than – biological storing and processing units, such as synapses and neurons.

Such elements do exist, and go under the name of *memristive*, *memcapacitive* and *meminductive systems*, or collectively simply named *memelements* [4]. These are resistors, capacitors and inductors, respectively, whose state at a given time depends on the history of applied inputs (e.g., charge, voltage, current, or flux) and states through which the system has evolved. As we have shown, these memelements provide an unifying description of materials and systems with memory [5], in the sense that all two-terminal electronic devices based on memory materials and systems, when subject to time-dependent perturbations, behave simply as – or as a combination of – memristive, memcapacitive and meminductive systems, namely, dynamical non-linear circuit elements with memory [6].

In this Chapter, we will show how the analog memory features of memelements are ideal to reproduce a host of processes typical of living organisms. We will review mainly work by the authors in various contexts, ranging from learning (adaptive) circuits to associative memory, and inherent massive parallelism afforded by networks of memelements. The Chapter is then organized as follows. Section 2 briefly reviews both the definition of these memory circuit elements and their main properties (a full account can be found in the original publications [7, 8, 4] and in our recent review paper [6]). Several experimental realizations exemplifying memristive, memcapacitive and meminductive systems are discussed in Sec. 3. Section 4 is devoted to biologically-inspired circuits based on memory circuit elements including simple adaptive circuits (Sec. 4.1), neuromorphic circuits (Sec. 4.2) and massively-parallel analog processing circuits (Sec. 4.3). Concluding remarks are given in Sec. 5.

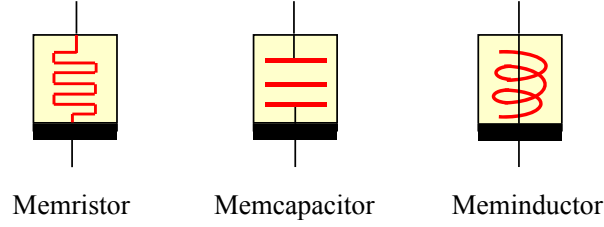


Fig. 1 Symbols of memory circuit elements: memristor, memcapacitor and meminductor. Generally, memelements are asymmetric devices. The thick horizontal lines above the bottom electrodes are employed to define the device polarity [4]. Reprinted with permission from Ref. [4]. ©2009 IEEE.

2 Definitions and properties

Let us consider electronic devices defined by all possible pairs of fundamental circuit variables $u(t)$ and $y(t)$ (i.e., current, charge, voltage, or flux). For each pair, we can introduce a response function, g , that, generally, depends on a set of n state variables, $x = \{x_i\}$, $i = 1, \dots, n$, describing the internal state of the system [4]¹. For instance, resistance of certain systems may depend on spin polarization [9, 10] or temperature [8]; capacitance and inductance of some other elements may exhibit dependence on system geometry [11, 6] or electric polarization [12]. In general, all internal microscopic physical properties related to the memory response of these electronic devices should be included into the vector of internal state variables x . The resulting memory circuit elements are then described by the following relations [4]

$$y(t) = g(x, u, t) u(t) \quad (1)$$

$$\dot{x} = f(x, u, t) \quad (2)$$

where f is a continuous n -dimensional vector function. Eqs. (1), (2) have to be supplied by appropriate initial conditions [13]. If u is the current and y is the voltage then Eqs. (1), (2) define memristive (for memory resistive) systems. In this case g is the *memristance* (memory resistance). In memcapacitive (memory capacitive) systems, the charge q is related to the voltage V so that g is the *memcapacitance* (memory capacitance). Finally, in meminductive (memory inductive) systems the flux φ is related to the current I with g the *meminductance* (memory inductance). There are still three additional pairs of fundamental circuit variables. However, these do not give rise to any new devices. For example, the pairs charge-current and voltage-flux are linked through equations of electrodynamics. Moreover, we could redefine devices defined by the charge-flux (which is the integral of the voltage) pair in the current-voltage basis [7]. Circuits symbols of memristive, memcapacitive and meminductive systems are presented in Fig. 1.

¹ There is no such dependence for traditional basic circuit elements – resistors, capacitors and inductors.

Let us consider memristive systems in more details (definitions of all the other elements can be easily derived by considering the different constitutive variables [4]). Specifically, a current-controlled memristive system [8, 4] is defined by Eqs. (1), (2) as

$$V_M(t) = R(x, I, t)I(t), \quad (3)$$

$$\dot{x} = f(x, I, t), \quad (4)$$

where $V_M(t)$ and $I(t)$ denote the voltage and current across the device, and R is the memristance. In a simple model of an ideal memristor [7], the memristance depends only on charge – the time integral of the current. One particular realization of such a model has been suggested in Ref. [14] and is formulated as

$$R_{ij}^M = R_{ON}x + R_{OFF}(1 - x), \quad (5)$$

where R_{ON} and R_{OFF} are minimal and maximal values of memristance, and x is a dimensionless internal state variable bound to the region $0 \leq x \leq 1$. The dynamics of x can then be simply chosen as [14]

$$\frac{dx}{dt} = \alpha I(t), \quad (6)$$

where α is a constant and $I(t)$ is the current flowing through the memristor.

Another example of memristive systems (which we will make use of later in this chapter) is a threshold-type memristive system [15]. Its model is specified by a threshold voltage (and some other parameters) that defines different device response regions (with regard to the voltage applied across the device). Mathematically, the threshold-type memristive system is described by the following equations

$$I = x^{-1}V_M, \quad (7)$$

$$\begin{aligned} \dot{x} = & (\beta V_M + 0.5(\alpha - \beta)[|V_M + V_t| - |V_M - V_t|]) \\ & \times \theta(x/R_1 - 1) \theta(1 - x/R_2), \end{aligned} \quad (8)$$

where I and V_M are the current through and the voltage drop on the device, respectively, and x is the internal state variable playing the role of memristance, $R = x$, $\theta(\cdot)$ is the step function, α and β characterize the rate of memristance change at $|V_M| \leq V_t$ and $|V_M| > V_t$, respectively, V_t is a threshold voltage, and R_1 and R_2 are limiting values of the memristance R . In Eq. (8), the θ -functions symbolically show that the memristance can change only between R_1 and R_2 . On a practical level, the value of x must be monitored at each time step and in the situations when $x < R_1$ or $x > R_2$, it must be set equal to R_1 or R_2 , respectively. In this way, we avoid situations when x may overshoot the limiting values by some amount and thus not change any longer because of the step function in Eq. (8). We have introduced and employed this model to describe the learning properties of unicellular organisms, associative memory, etc., as we will describe in some detail in the following sections.

There are several properties that characterize memory circuit elements. We refer the reader to the original papers [7, 8, 4] and the extensive review [6] where these are discussed at length. Here, we just mention that they are typically characterized by a frequency-dependent "pinched hysteresis loop" in their constitutive variables when subject to a periodic input. Also, normally, the memristance, memcapacitance and meminductance acquire values between two limits (with exceptions as discussed in Refs. [6, 12, 16]). Although the hysteresis of these elements under a periodic input may strongly depend on initial conditions [13], it is generally more pronounced at frequencies of the external input that are comparable to frequencies of internal processes that lead to memory. In many cases, at very low frequencies memory circuit elements behave as non-linear elements while at high frequencies as linear elements.

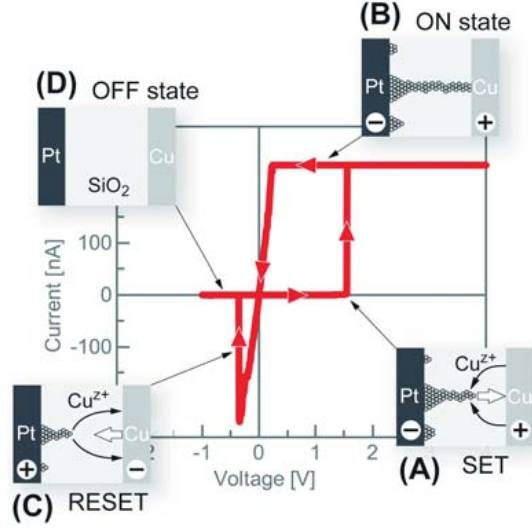
Also, the hysteresis loops may or may not show self-crossing - which we have named type-I and type-II crossing behavior, respectively [6] - and often the internal state variable remains unchanged for a long time without any input signal applied. This provides non-volatile memory, which is an important feature for some of the applications we discuss later.

Finally, we mention that the state variables - whether from a continuum or a discrete set of states - may follow a *stochastic differential equation* rather than a deterministic one [6]. Interesting effects have been predicted in the presence of noise, such as noise-induced hysteresis [17]. This may have a large bearing in simulating biological processes - which necessarily occur under noisy conditions - and could be used to enhance the performance of certain devices.

3 Experimental realizations

In this section, we briefly discuss experimental realizations of memory circuit elements. There is a large amount of experimental systems showing memristive behavior (based, however, on very different physical mechanisms). For example, in thermistors - being among the first identified memristive systems [8] - the memory effects are related to thermal effects, mainly on how fast the heat dissipation occurs. In spintronics memristive systems, either based on semiconductor [9] or metal [10] materials, the memory feature is provided by the electron spin degree of freedom. Finally, resistance switching memory cells are probably the most important type of memristive systems. These cells are normally built of two metal electrodes separated by a gap of a few tens of nanometers filled by a memristive material. Different physical processes inside the memristive material can be responsible for the memory. Fig. 2 shows an example of resistance switching memory cell - an electrochemical metallization cell - in which a layer of dielectric material (SiO_2) separates two dissimilar metal electrodes (made of copper and platinum) [18]. Externally applied voltage induces migration of copper atoms that can bridge the gap between the electrodes thus reducing the cell's resistance. Such a bridge can also be disrupted by the applied voltage of the opposite polarity (see Fig. 2).

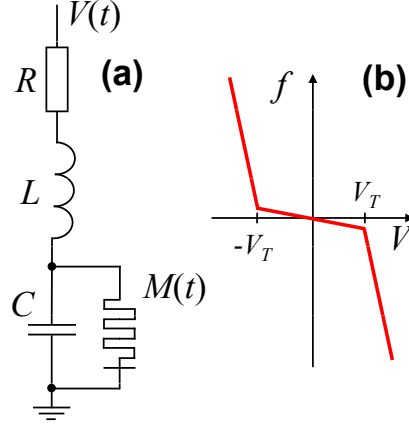
Fig. 2 Current-voltage characteristic of a Cu/SiO₂/Pt electrochemical metallization cell recorded using a triangular voltage sweep. The insets show dynamics of metallic filament formation. (Reprinted with permission from [18]. 2009 American Institute of Physics.)



Memcapacitive effects can be related to changes in the capacitor geometry or specific intrinsic properties of dielectric medium located between the capacitor plates [6]. For instance, the former mechanism plays the main role in elastic memcapacitive systems that could be based on internal elastic states of the capacitor plate (e.g., direction of bending [11]) or elasticity of a medium between the plates that could be thought of as a spring [6]. Examples of the latter mechanism include memcapacitive systems with a delayed polarization response [12, 16] and structures with permittivity switching [19]. Although meminductive systems are the least studied memory circuit elements at the moment, there are several known systems showing such type of functionality. For instance, in bimorph meminductive systems [20, 21, 22], the inductance depends on the inductor's shape defined by the inductor temperature. Heat dissipation mechanisms play a significant role in this type of systems. Many additional examples of memristive, memcapacitive and meminductive systems can be found in our recent review paper [6]. The most important aspect of all these examples is that they relate primarily to structures with nanoscale dimensions. This is not surprising since (up to a certain limit) the smaller the dimensions of the system the easier it is to observe memory effects.

In addition, we would like to mention that several types of memory effects may be present in a single device. For example, the coexistence of memristive and memcapacitive responses has been observed in perovskite oxide thin films [23]. Moreover, several three-terminal transistor-like memristive devices have been investigated in the past [24, 25, 26]. Clearly, different types of memory materials can be combined to obtain multi-terminal device structures with complex functionalities.

Fig. 3 (a) A possible realization of the learning circuit consisting of resistor R , inductor L , capacitor C and memristive system M . (b) Schematics of the function $f(V)$ defining a threshold-type memristive system (see also Eqs. (7), (8)). Reprinted with permission from Ref. [15]. ©2009 American Physical Society.



4 Biologically-Inspired Circuits

4.1 Modeling adaptive behavior of unicellular organisms

Adaptive behavior is common to all life forms on Earth of all five kingdoms of nature: in Plantae (the plants) [27, 28, 29], Animalia (the animals) [30], Protista (the single-celled eukaryotes) [31, 32], Fungi (fungus and related organisms) [33, 34], and Monera (the prokaryotes) [35, 36, 37]. (The literature on this subject is extensive, hence we have given only a few representative references.) To a greater or lesser extent, representatives of all life forms respond (adapt) to changes of their environment in a manner that increases the survival of their species. It would thus be of benefit to mimic and use this important natural feature in artificial structures, in particular in electronics to allow novel functionalities otherwise nonexistent in standard circuitry. There are indeed many domains where such *learning circuits* can be employed. These range from robot control systems to signal processing. Therefore, developing circuit models of the adaptive behavior of the natural world is of great importance in many scientific areas [38]. Note that by "learning" here we simply mean the ability to adapt to incoming signals with retention of such information for later use.

In this section we consider a particularly interesting example: the ability of the slime mold *Physarum polycephalum* to adapt its locomotion to periodic changes of the environment [32]. The simplicity of the system - a unicellular organism - and its well-defined response to specific input signals, make it an ideal test bed for the application of the notion of memory circuit elements in biology, and a source of inspiration for more complex adaptive behavior in living organisms. In addition, this is a particularly appealing example of the full range of properties of memelements, in particular, their *analog* capability, which expands their range far beyond the digital domain.

In particular, it has been shown in a recent experiment [32] that the *Physarum polycephalum* subjected to periodic unfavorable environmental conditions (lower temperature and humidity) not only responds to these conditions by reducing its locomotion speed, but also anticipates future unfavorable environmental conditions reducing the speed at the time when the next unfavorable episode would have occurred. While the microscopic mechanism of such behavior has not been identified by the authors of that work [32], their experimental measurements clearly prove the ability of *Physarum polycephalum* to anticipate an impending environmental change.

More specifically, the locomotion speed of the *Physarum polycephalum* was measured when favorable environmental conditions (26°C and 90% humidity) were interrupted by three equally spaced 10 min pulses of unfavorable environmental conditions (22°C and 60% humidity) [32]. The time separation between the pulses τ was selected between 30 and 90 minutes. It was observed that the locomotion speed at favorable conditions (approximately 0.25 mm/10min as shown in Fig. 1 of Ref. [32]) turns to close to zero each time the unfavorable conditions were presented. However, *spontaneous in-phase slow downs* were observed after time intervals τ , 2τ and even 3τ after the last application of unfavorable conditions. In addition, if – after a long period of favorable conditions – a single pulse of unfavorable conditions is applied again then a spontaneous slow down (called a *spontaneous in-phase slow down after one disappearance* [32]) after a time interval τ was observed. It clearly follows from this experiment that the *Physarum polycephalum* has a mechanism to memorize (“learn”) the periodicity of environmental changes and adapts its behavior in anticipation of next changes to come [32].

We have developed a circuit model [15] of the adaptive behavior of the slime mold which has been later realized experimentally [39] using vanadium dioxide as memory element [40, 41]. The learning circuit is shown in Fig. 3(a). Here, the role of environmental conditions is played by the input voltage $V(t)$ and the speed of locomotion is mapped into the voltage across the capacitor C . The learning circuit design resembles a damped LC contour in which the amount of damping is controlled by the state of the memristive system M . To understand the circuit operation, we note that the memristive system employed in the circuit is of a threshold type (see Eqs. (7) and (8)), namely, its state can be significantly changed only by a voltage (across the memristive system) with a magnitude exceeding a certain threshold. Fig. 3(b) presents the switching function $f(V)$ used to describe a threshold-type memristive system.

Our simulations of the learning circuit response to irregular and regular sequences of pulses are shown in Fig. 4. In these simulations, the scheme described above has been used with the only restriction that the response signal cannot exceed a certain value [15] (electronically, a cut-off can be easily obtained by using an additional resistor and diode). When an irregular sequence of pulses is applied to the circuit, the voltage oscillations across the capacitor can not exceed the threshold voltage of the memristive system M which continues to stay in its initial low-resistance state, thus damping the circuit. When the pulses are applied periodically with a period close to the period of the LC contour oscillations, a sufficiently strong voltage

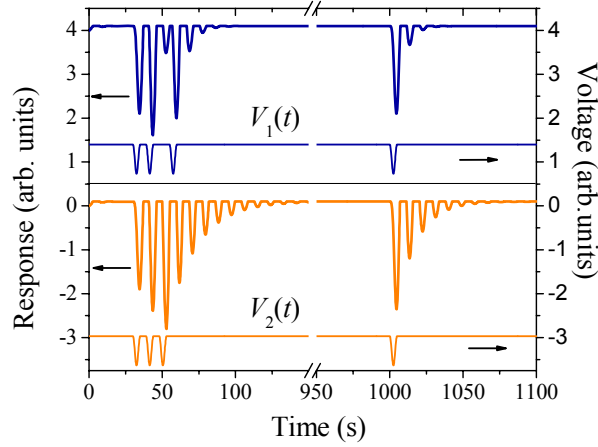


Fig. 4 Modeling of the spontaneous in-phase slow-down responses [15]. This plot demonstrates that stronger and longer-lasting responses for both spontaneous in-phase slow down and spontaneous in-phase slow down after one disappearance of the stimulus are observed only when the circuit was previously trained by a periodic sequence of three equally spaced pulses as present in $V_2(t)$. The applied voltage $V_1(t)$ is irregular and thus the three first pulses do not “train” the circuit. Reprinted with permission from Ref. [15]. ©2009 American Physical Society.

across the capacitor C is induced. This voltage switches the memristive system into the high-resistance state. Therefore, in this case, oscillations in the contour are less damped and last longer as Fig. 4 demonstrates. These oscillations exactly model the spontaneous in-phase slow down and in-phase slow down after one disappearance effects observed experimentally [32]. We note that a single learning circuit memorizes past events of a frequency close to the resonance frequency of LC contour. An array of learning circuits would model the learning of *Physarum polycephalum* in the whole frequency range [15].

Recently, an experimental implementation of this learning circuit has been reported [39]. In this work, a learning circuit similar to that in Fig. 3(a) has been built with the only difference that the memristive system (a vanadium dioxide memristive device [39]) has been connected in series with a capacitor (Fig. 5(a)). The memristive properties of vanadium dioxide are based on an insulator-to-metal phase transition occurring in this material in the vicinity of 342K [40, 41]. In order to realize the memristive functionality, the vanadium dioxide device is heated to a steady-state temperature of 339.80 K (right below the transition temperature) and subjected to an externally applied voltage. The Joule heating (due to the applied voltage) incrementally drives the vanadium dioxide material through the phase transition, thus reducing its resistance. The operation of the learning circuit depicted in Fig. 5(a) is then clear. While off-resonance signals applied to the circuit can not excite a sufficient current to drive the vanadium dioxide through the phase transition, the current generated by resonance signals is sufficient for this purpose. Fig. 5(b) demonstrates modification of the transfer function of the circuit caused by off-resonance and res-

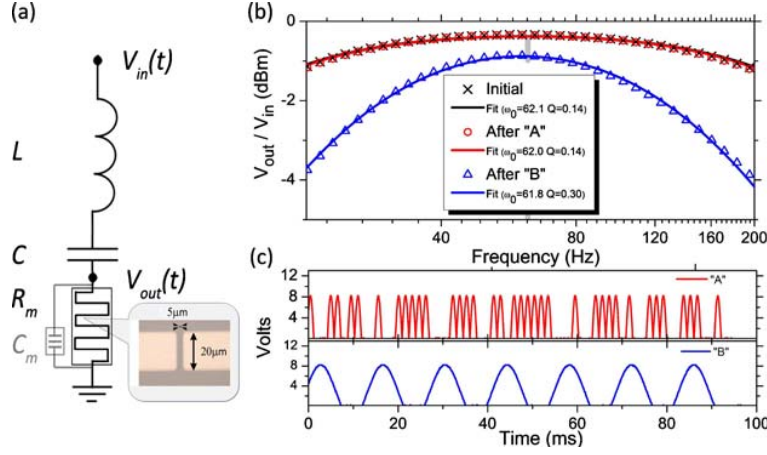


Fig. 5 Experimental realization of the learning circuit (adaptive filter) based on vanadium dioxide memristive device. (a) Schematic of the adaptive filter in which the memristive device (with a small memcapacitive component) is connected in series with a capacitor C and inductor L . We note that such realization of the learning circuit operates similarly to the learning circuit shown in Fig. 3(a). (b) Small-signal (10 mV) transfer function (V_{out}/V_{in}) for the adaptive filter plotted before and after off-resonance "A" and on-resonance "B" pulses. Solid lines are RLC bandpass-filter fit to data, which generates the ω_0 and Q values in the legend. Pulse sequence B has a significant training effect on the circuit, while A has little or no effect. (c) Time series of the off-resonance "A" sequence of pulses and on-resonance "B" sequence of pulses. Reprinted with permission from Ref. [39]. ©2010 American Institute of Physics.

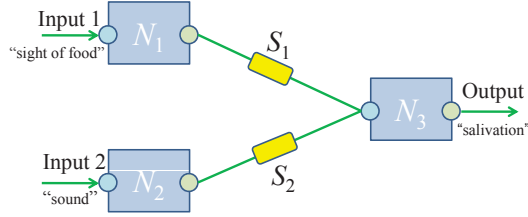
onance pulse sequences (Fig. 5(c)) applied to the circuit. Fig. 5(b) clearly indicates a change in the transfer function caused by resonance signals (learning).

Finally, we mention that the formalism of memory circuit elements [4] has also been useful in modeling biophysical systems whose electric response depends on the history of applied voltages or currents. An example of such situation is the electro-osmosis in skin which has been recently described by a memristive model [42]. Physically, the voltage applied to the skin induces a water flow in sweat-duct capillaries changing the skin conductance. The position of the water table (the level separating dry and wet zones) in capillaries plays the role of the internal state variable whose dynamics is determined by the applied voltage [42]. The memristive model of electro-osmosis [42] is in a good agreement with experimental data and further demonstrates the potential of the formalism of memory circuit elements for modeling biophysical processes.

4.2 Neuromorphic circuits

Our second example of biologically-inspired circuits with memory circuit elements is from the area of neural networks. Neural networks form a class of circuits whose

Fig. 6 Memristive neural network with an associative memory ability. Here, two input neurons (N_1 and N_2) are connected through memristive synapses (S_1 and S_2) to the output neuron N_3 . The details of circuit operation are given in the text. Reprinted from Ref. [44]. ©2010 with permission from Elsevier.



operation mimics the operation of the human (and animal) brain. Below, we consider electronic implementations of two important processes occurring in biological neural networks: associative memory and spike timing-dependent plasticity. Both features can be implemented in artificial neural networks based on memristive synapses.

4.2.1 Associative memory

The associative memory is one of the most fundamental functionalities of the human (and animal) brain. By making associations we learn, adapt to a changing environment and better retain and recall events. One of the most famous experiments related to associative memory is Pavlov's experiment [43] whereby salivation of a dog's mouth is first set by the sight of food. Then, if the sight of food is accompanied by a sound (e.g., the tone of a bell) over a certain period of time, the dog learns to associate the sound to the food, and salivation can be triggered by the sound alone, without the intervention of vision.

Recently, we have reproduced [44] the Pavlov's experiment utilizing a neural network with memristive synapses. As a first example, we have implemented the well known Hebbian rule introduced by Hebb in 1949: "when an axon of cell A is near enough to excite a cell B and repeatedly or persistently takes part in firing it, some growth process or metabolic change takes place in one or both cells such that A's efficiency, as one of the cells firing B, is increased" [45]. To put it differently, the neurons that fire together, wire together.

In order to show associative memory, let us consider a simple neural network consisting of three electronic neurons and two memristive synapses as shown in Fig. 6. We assume that the first input neuron activates under a specific ("visual") event, such as "sight of food", and the second input neuron activates under another ("auditory") event, such as a particular "sound".

On the electronic level, an electronic neuron sends forward (to its output) and backward (to its input) voltage spikes of opposite polarity when the amplitude of the input signal exceeds a threshold value. Regarding the dynamics of memristive synapses, they have been selected of a threshold-type (Eqs. (7) and (8)) with a threshold voltage exceeding the output voltage of electronic neurons. In this case,

voltage spikes applied to a single terminal of a memristive synapse is not enough to induce its change. The latter is possible only if forward and backward propagating spikes overlap in time across a synapse. We have employed memristor emulators [46, 44] as memristive synapses². The main components of a memristor emulator are a digital potentiometer, a microcontroller and an analog-to-digital converter. Using the converter, the microcontroller continuously reads the voltage applied to the digital potentiometer and updates the potentiometer resistance according to a pre-programmed model of a voltage- or current-controlled memristive system. The operation of electronic neurons is realized along similar lines [44]. Operation of the associative memory is presented in Fig. 7 where a detail of this process is given.

Our work as described above [44] demonstrates the potential of memristive devices for neuromorphic circuits applications. Importantly, it has been recently shown in numerous experiments that memristive devices can be built at the nanoscale [52, 53, 54, 55, 56, 57, 14, 58, 59, 18, 60, 6, 61, 62]. This opens up the possibility to

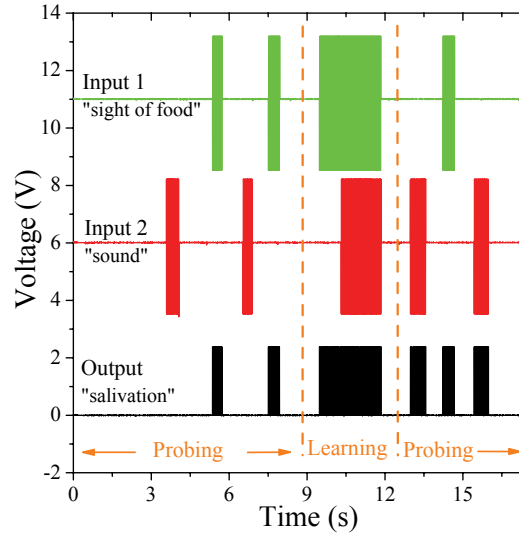


Fig. 7 Experimental demonstration of the associative memory with memristive neural networks. In this experiment, a simple neural network shown in Fig. 6 was realized. The first "probing" phase demonstrates that, initially, only a signal from N_1 neuron activates the output neuron. The association of the Input 2 signal with the Output develops in the "learning phase" when N_1 and N_2 neurons are simultaneously activated. In this case, a signal at the Input 1 excites the third neuron that sends back-propagating pulses of a negative amplitude. These pulses, when applied simultaneously with forward propagating pulses from the Input 2 to the second memristive synapse S_2 cause it to learn. The final "probing" phase demonstrates that signals from both N_1 and N_2 activate the output neuron. A detailed description of the experiment is given in Ref. [44]. Reprinted from Ref. [44]. ©2010 with permission from Elsevier.

² Several designs of memristor [46, 47, 48, 7] as well as memcapacitor and meminductor [47, 49, 50, 51] emulators are known in the literature. These emulators serve as an important practical tool to build small-scale circuits with memory circuit elements.

fabricate neuromorphic circuits with the same amount of memristive synapses as the number of biological synapses in the human brain ($\sim 10^{14}$). In fact, one of the main challenges for practical realizations of an artificial brain on a chip is related to the high connectivity of biological neurons. It has been estimated that, on average, the number of connections per neuron is of the order of 10^3 . Therefore, neural networks of memelements built at the nanoscale offer advantages - in terms of density - unavailable with current active elements (such as transistors).

4.2.2 Spike timing-dependent plasticity

However, the above mentioned simple Hebbian rule does not describe the much more complicated time-dependent plasticity of biological synapses [63, 64, 65, 66]. The latter has come to be known as spike timing-dependent plasticity (STDP). When a post-synaptic signal reaches the synapse *before* the action potential of the pre-synaptic neuron, the synapse shows long-term depression (LTD), namely its strength decreases (smaller connection between the neurons) depending on the time difference between the post-synaptic and the pre-synaptic signals. Conversely, when the post-synaptic action potential reaches the synapse *after* the pre-synaptic action potential, the synapse undergoes a long-time potentiation (LTP), namely the signal transmission between the two neurons increases in proportion to the time difference between the pre-synaptic and the post-synaptic signals. The learning process and the storing of information in the brain thus follow non-trivial time-dependent features which have not been fully understood yet. Implementation of STDP in artificial networks can thus help unraveling these mechanisms.

The spike timing-dependent plasticity can be implemented using different types of memristive systems. Following our previous work [67], neuromorphic circuits can be based on memristive systems with or without an internal spike-timing tracking capability. In the most simple case, memristive systems without spike-timing tracking capability are of the first order, while those supporting such capability are of the second order as an additional internal state variable is needed to track timing of pre-synaptic and post-synaptic pulses [67]. In the first case, an additional external hardware is required to implement the spike timing-dependent plasticity. For example, STDP was recently realized using a combination of memristive systems with CMOS (complementary metal-oxide-semiconductor) elements [60] (see Fig. 8). Another approach involves utilization of overlapping pulses of opposite polarities [67, 68, 69].

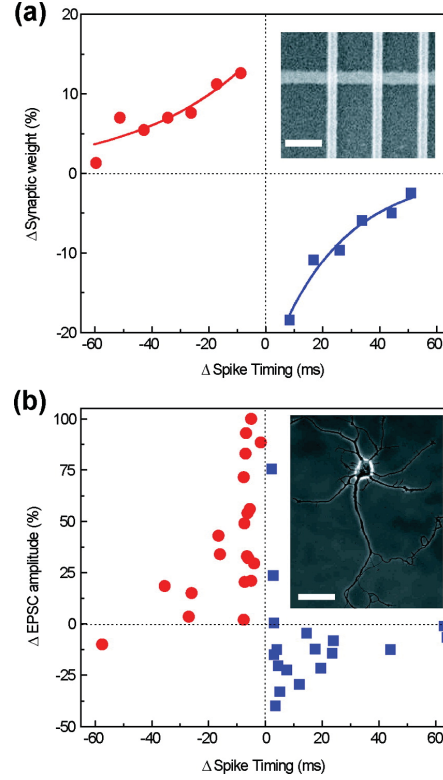
A simple second-order memristive system with time-tracking capability is described by the following equations [67]

$$R = x, \quad (9)$$

$$\dot{x} = \gamma[\theta(V_M - V_t)\theta(y - y_t) + \theta(-V_M - V_t)\theta(-y - y_t)]y, \quad (10)$$

$$\dot{y} = \frac{1}{\tau}[-V_M\theta(V_M - V_t)\theta(y_t - y) - V_M\theta(-V_M - V_t)\theta(y + y_t) - y], \quad (11)$$

Fig. 8 (a) Measured change in the synaptic weight versus spike separation. Inset: SEM image of the memristive crossbar array, scale bar is 300 nm. (b) Measured change in excitatory postsynaptic current of rat neurons after repetitive correlated spiking versus relative spiking timing (the plot was reconstructed from Ref. [65]). Inset: image of a hippocampal neuron (the image was adapted with permission from reference [70]). Scale bar is 50 μm . Reprinted with permission from [60]. Copyright 2010 American Chemical Society.



where x and y are internal state variables, γ is a constant, V_t is a threshold voltage, y_t is the threshold value of y , and τ is a constant defining the time window of STDP. The second-order memristive system with timing tracking capability defined by the above equations is very promising for neuromorphic circuits application since neuron's firing can be implemented simply by short single rectangular pulses and no additional hardware as in the case of first-order memristors (see, e.g., Ref. [60]). However, such solid-state second-order memristors need to be developed, even though their implementation in memristor emulators [46, 47] can be easily realized.

Moreover, several authors have discussed applications of three-terminal transistor-like electronic devices with memory [25, 26, 71] in the area of neuromorphic computing. Although, formally such devices can not be categorized as memristive systems, their operation is clearly based on memristive effects. In particular, Lai *et al.* [26] have experimentally fabricated a synaptic transistor. For instance, Fig. 9 depicts their experimental scheme and selected measurement results that confirm realization of spike timing-dependent plasticity in this device.

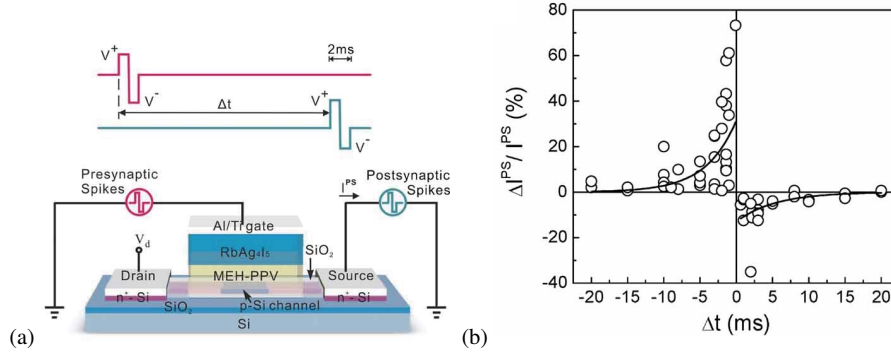


Fig. 9 (a) Structure of synaptic transistor . (b) The relative changes of the postsynaptic currents measured after application of 120 pairs of temporally correlated pre- and post-synaptic spikes. From [26], copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission.

4.3 Networks of memory circuit elements

A human brain - and also the brain of many other living organisms - solves many problems much better than traditional computers. The reason for this is a type of massive parallelism in which a large number of neurons and synapses participate simultaneously in the calculation. Here, we consider networks of memory circuit elements and their ability to *i*) solve efficiently certain graph theory optimization problems, and *ii*) retain such information for later use. In particular, we demonstrate that a network of memristive devices solves the maze problem much faster than any existing algorithm [72]. Similar to the brain's operation, such an extraordinary advance in computational power is due to the massively-parallel network dynamics in which all network components are simultaneously involved in the calculation. This type of parallelism could be dubbed as an *analog parallelism* which is very different from that used in conventional supercomputers. In the latter systems, each core typically runs a separate process that, relatively rarely, exchanges information with other cores. In calculations done by networks, the information exchange is continuous resulting in a tremendous increase of computational power as we demonstrate below.

Left panel of Fig. 10 depicts a memristive network (memristive processor) in which points of a square grid are connected by basic units (memristive system plus switch (FET)) [72]. Each switch in the network can be in the "connected" or "not-connected" state. Since the direction of current flow in the network is not known *a priori*, the polarity of adjacent memristive devices (indicated by the black thick line in the memristor symbol in Figure 1) is chosen to be alternating. Experimentally, the suggested network could be fabricated using, e.g., CMOL (Cmos+MOlecular-scale devices) architecture [73] combining a single memristor layer with a conventional CMOS layer. The operation of the massively-parallel processor consists of three

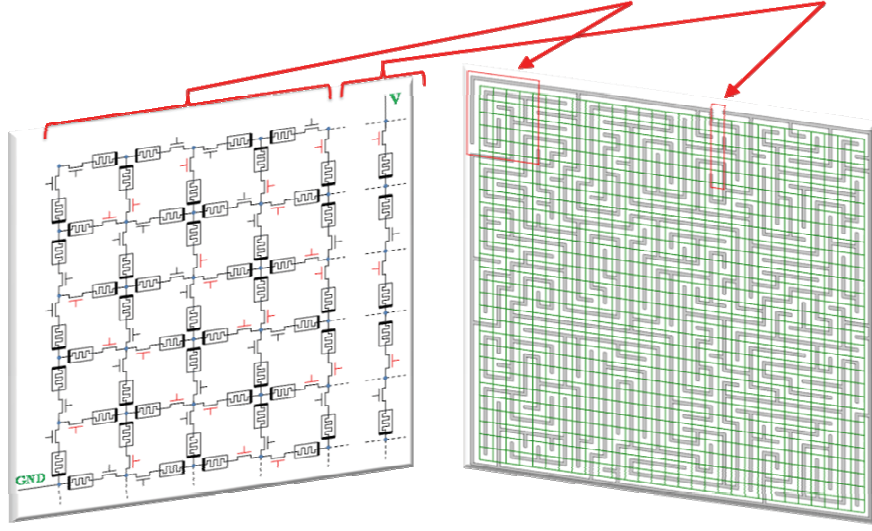


Fig. 10 Maze mapping into a network of memristors. *Right panel.* The maze is covered by an array of vertical and horizontal lines having the periodicity of the maze. *Left panel.* Architecture of the network of memristors in which each crossing between vertical and horizontal lines in the array (in the right panel) is represented by a grid point to which several basic units consisting of memristors and switches (field-effect transistors) are linked in series. The maze topology is encoded into the state of the switches such that if the short line segment connecting neighboring crossing points in the array crosses the maze wall then the state of the corresponding switch is "not connected" (shown with red symbols). All other switches are in the "connected" state. The external voltage (V) is applied across the connection points corresponding to the entrance (V) and exit (ground, GND) points of the maze. Reprinted with permission from Ref. [72]. ©2011 American Physical Society.

main stages: initialization, computation and reading out the computation result. All these stages are realized by externally applied signals (originating, e.g., from the CMOS layer).

During the first initialization stage, all memristive elements in the network are switched into the "OFF" state. This can be done, for example, by applying GND and appropriately selected V_1 voltages in a chessboard-like pattern to all grid points of the memristive network for a sufficiently long period of time [72]. After that, the maze topology is mapped onto the memristive network by setting appropriate switches into the "not connected" state. We describe this process in the caption of Fig. 10. The computation stage consists in the application of a single voltage pulse of appropriate amplitude and duration across grid points corresponding to the entrance and exit points of the maze. The solution can be later read or used in further calculations.

We have modeled the memristive processor operation by numerically solving Kirchhoff's current law equations complemented by Eqs. (5), (6) which in the present network case are modified as

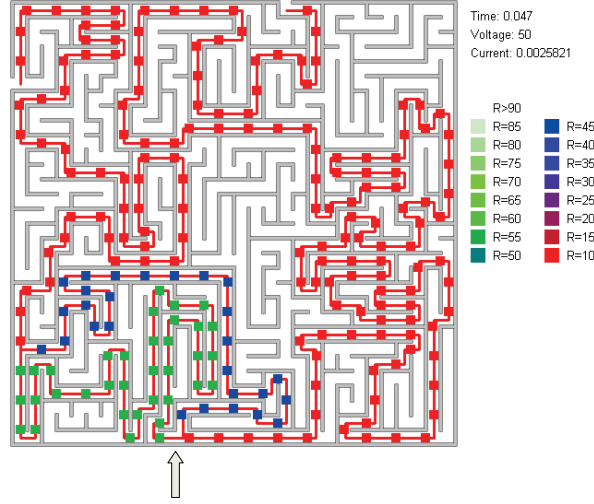


Fig. 11 Solution of a multiple-path maze [72]. The maze solution contains two common segments (red dots connected by a red line), and two alternative segments of different lengths close to the left bottom corner. The memristance in the shorter segment (blue dots connected by a red line) is smaller than that in the longer segment (green dots connected by a red line) since the current through the shorter segment is larger and, consequently, the change of the memristors' state along this segment is larger. The arrow at the bottom indicates a splitting point of the solution path. The resistance is in Ohms, the voltage is in Volts and the current is in Amperes. Reprinted with permission from Ref. [72]. ©2011 American Physical Society.

$$R_{ij}^M = R_{ON}x_{ij} + R_{OFF}(1 - x_{ij}), \quad (12)$$

where R_{ON} and R_{OFF} are again the minimal and maximal values of memristance, x_{ij} is the dimensionless internal state variable for each memristor bound to the region $0 \leq x_{ij} \leq 1$, and (i, j) are grid indexes of a memristor to identify its location in the network. The dynamics of x_{ij} is then given by

$$\frac{dx_{ij}}{dt} = \alpha I_{ij}(t), \quad (13)$$

with α a constant and $I_{ij}(t)$ the current flowing through the memristor (ij) .

Fig. 11(a) shows a solution of a multiple-path maze. The maze solution is clearly seen in Fig. 11 as chains of red, blue and green boxes (representing memristive devices with lower memristance) connected by a red line. Importantly, the memristive processor not only determines all possible solutions of the maze but also stores them and sorts them out according to their length. This feature is described in more details in the caption of Fig. 11. Also, the memristive processor requires only *one single step* to find the maze solution thus outperforming all known maze solving approaches and algorithms.

We also note that the wide selection of physical mechanisms of memory we can "shop" from, offers many opportunities to design novel efficient electronic devices [6]. For example, a memristive processor based on fast switching nanoionic metal/insulator/metal cells [6] would require just few nanoseconds or even less³ to solve the maze. More generally, a network of memristors - or other memory circuit elements - can be considered as an adaptable medium whose state dynamically changes in response to time-dependent signals or changes in the network configuration. Therefore, the use of these processors is not limited to maze solving: We expect they could help find the solution of many graph theory optimization problems including, for instance, the traveling salesman problem, shortest path problem, etc.

5 Conclusions and Outlook

In conclusion, we have shown that the two-terminal electronic devices with memory – memristive, memcapacitive and meminductive systems – are very useful to model a variety of biological processes and systems. The electronic implementation of all these mechanisms can clearly lead to a novel generation of "smart" electronic circuits that can find useful applications in diverse areas of science and technology. In addition, these memelements and their networks, provide solid ground to test various hypothesis and ideas regarding the functioning of the human (and animal) brain both theoretically and experimentally. Theoretically because their flexibility in terms of what type and how many internal state variables responsible for memory, or what network topology are required to reproduce certain biological functions can lead to a better understanding of the microscopic mechanisms that are responsible for such features in living organisms. Experimentally because with the continuing miniaturization of electronic devices, memelements can be assembled into networks with similar densities as the biological systems (e.g., the brain) they are designed to emulate. In particular, we anticipate potential applications for memcapacitive and meminductive systems [4] which offer such an important property as low energy dissipation combined with information storage capabilities. We are thus confident that the area of biologically-inspired electronics with memory circuit elements will offer many research opportunities in several fields of science and technology.

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³ Fast sub-nanosecond switching has been recently reported in tantalum oxide memristive systems [62].

References

1. S.J. Russell, P. Norvig, *Artificial Intelligence: A Modern Approach*, 3rd edn. (Prentice Hall, 2009)
2. A. Colorni, M. M. Dorigo, V. Maniezzo, in *Actes de la premiere conference europeenne sur la vie artificielle, Paris, France, Elsevier Publishing* (1991), pp. 134–142
3. N. Monmarche, F. Guinand, P. Siarry, *Artificial Ants* (Wiley-ISTE, 2010)
4. M. Di Ventra, Y.V. Pershin, L.O. Chua, *Proc. IEEE* **97**(10), 1717 (2009)
5. M. Di Ventra, Y.V. Pershin, *Mat. Today* **14**, 584 (2011)
6. Y.V. Pershin, M. Di Ventra, *Advances in Physics* **60**, 145 (2011)
7. L.O. Chua, *IEEE Trans. Circuit Theory* **18**, 507 (1971)
8. L.O. Chua, S.M. Kang, *Proc. IEEE* **64**, 209 (1976)
9. Y.V. Pershin, M. Di Ventra, *Phys. Rev. B* **78**, 113309 (2008)
10. X. Wang, Y. Chen, H. Xi, H. Li, D. Dimitrov, *El. Dev. Lett.* **30**, 294 (2009)
11. J. Martinez-Rincon, Y.V. Pershin, *IEEE Trans. El. Dev.* **58**, 1809 (2011)
12. J. Martinez-Rincon, M. Di Ventra, Y.V. Pershin, *Phys. Rev. B* **81**, 195430 (2010)
13. F. Corinto, A. Ascoli, M. Gilli, submitted for publication (2011)
14. D.B. Strukov, G.S. Snider, D.R. Stewart, R.S. Williams, *Nature* **453**, 80 (2008)
15. Y.V. Pershin, S. La Fontaine, M. Di Ventra, *Phys. Rev. E* **80**, 021926 (2009)
16. M. Krems, Y.V. Pershin, M. Di Ventra, *Nano Lett.* **10**, 2674 (2010)
17. A. Stotland, M. Di Ventra, arXiv:1104.4485v2 (2011)
18. C. Schindler, G. Staikov, R. Waser, *Appl. Phys. Lett.* **94**, 072109 (2009)
19. Q. Lai, L. Zhang, Z. Li, W.F. Stickle, R.S. Williams, Y. Chen, *Appl. Phys. Lett.* **95**, 213503 (2009)
20. V. Lubecke, B. Barber, E. Chan, D. Lopez, M. Gross, P. Gammel, *IEEE Trans. Microw. Theory Tech.* **49**(11), 2093 (2001)
21. I. Zine-El-Abidine, M. Okoniewski, J.G. McRory, in *Proceedings of the 2004 International Conference on MEMS, NANO and Smart Systems (ICMENS'04)* (2004), pp. 636–638
22. S. Chang, S. Sivoththaman, *IEEE El. Dev. Lett.* **27**(11), 905 (2006)
23. S. Liu, N. Wu, A. Ignatiev, J. Li, J. Appl. Phys. **100**, 056101 (2006)
24. V.V. Erokhin, T.S. Berzina, M.P. Fontana, *Crystallogr. Rep.* **52**, 159 (2007)
25. F. Alibert, S. Pleutin, D. Guerin, C. Novembre, S. Lenfant, K. Lmimouni, C. Gamrat, D. Vuillaume, *Adv. Funct. Mat.* **20**, 330 (2010)
26. Q. Lai, L. Zhang, Z. Li, W.F. Stickle, R.S. Williams, Y. Chen, *Adv. Mat.* **22**, 2448 (2010)
27. T. Kozłowski, S. Pallardy, *Botanical Review* **68**, 270 (2002)
28. A. Trewavas, *Annals of Botany* **92**, 1 (1998)
29. P. Calvo Garzon, F. Keijzer, *Adaptive Behavior* **19**, 155 (2011)
30. J.E.R. Staddon, *Adaptive behavior and learning* (Cambridge University Press, 1983)
31. J. Ojal, *Biol. Cybern.* **79**, 403 (1998)
32. T. Saigusa, A. Tero, T. Nakagaki, Y. Kuramoto, *Phys. Rev. Lett.* **100**, 018101 (2008)
33. Q. Li, B. McNeil, L.M. Harvey, *Free Radical Biology and Medicine* **44**, 394 (2008)
34. J. Hartley, J.W.G. Cairney, A.A. Meharg, *Plant and Soil* **189**, 303 (1997)
35. H. Thieringer, P. Jones, M. Inouye, *BioEssays* **20**, 49 (1998)
36. J. van der Oost, M.M. Jore, E.R. Westra, M. Lundgren, S.J.J. Brouns, *Trends in Biochemical Sciences* **34**, 401 (2009)
37. J. Larsson, J.A.A. Nylander, B. Bergman, *BMC evolutionary biology* **11**, 187 (2011)
38. J.H. Holland, *Adaptation in Natural and Artificial Systems: An Introductory Analysis with Applications to Biology, Control, and Artificial Intelligence* (Bradford Book, 1992)
39. T. Driscoll, J. Quinn, S. Klein, H.T. Kim, B.J. Kim, Y.V. Pershin, M. Di Ventra, D.N. Basov, *Appl. Phys. Lett.* **97**, 093502 (2010)
40. T. Driscoll, H.T. Kim, B.G. Chae, M. Di Ventra, D.N. Basov, *Appl. Phys. Lett.* **95**, 043503 (2009)
41. T. Driscoll, H.T. Kim, B.G. Chae, B.J. Kim, Y.W. Lee, N.M. Jokerst, S. Palit, D.R. Smith, M. Di Ventra, D.N. Basov, *Science* **325**, 1518 (2009)

42. G.K. Johnsen, C.A. Lütken, O.G. Martinsen, S. Grimnes, *Phys. Rev. E* **83**, 031916 (2011)
43. I. Pavlov, *Conditioned Reflexes: An Investigation of the Physiological Activity of the Cerebral Cortex* (London: Oxford University Press, 1927). (translated by G. V. Anrep)
44. Y.V. Pershin, M. Di Ventra, *Neural Networks* **23**, 881 (2010)
45. D.O. Hebb, *The Organization of Behavior; A Neuropsychological Theory* (New York: Wiley, 1949)
46. Y.V. Pershin, M. Di Ventra, *IEEE Trans. Circ. Syst. I* **57**, 1857 (2010)
47. D. Biolek, V. Biolkova, *Int. J. Numer. Mod.* (in press) (2011)
48. D. Biolek, V. Biolkova, Z. Kolka, in *5th International Conference on Circuits, Systems and Signals (CSS'11)*. (2011), p. 171
49. D. Biolek, V. Biolkova, *El. Lett.* **46**, 1428 (2010)
50. Y.V. Pershin, M. Di Ventra, *El. Lett.* **47**, 243 (2011)
51. Y.V. Pershin, M. Di Ventra, *El. Lett.* **46**, 517 (2010)
52. T. Tamura, T. Hasegawa, K. Terabe, T. Nakayama, T. Sakamoto, H. Sunamura, H. Kawaura, S. Hosaka, M. Aono, *Jpn. J. Appl. Phys.* **45**, L364 (2006)
53. R.R. Waser, M. Aono, *Nat. Mat.* **6**, 833 (2007)
54. D. Lee, D. jun Seong, I. Jo, F. Xiang, R. Dong, S. Oh, , H. Hwang, *Appl. Phys. Lett.* **90**, 122104 (2007)
55. S. Dietrich, M. Angerbauer, M. Ivanov, D. Gogl, H. Hoenigschmid, M. Kund, C. Liaw, M. Markert, *IEEE J. Sol.-State Circ.* **42**, 839 (2007)
56. S. Raoux, G.W. Burr, M.J. Breitwisch, C.T. Rettner, Y.C. Chen, R.M. Shelby, M. Salinga, D. Krebs, S.H. Chen, H.L. Lung, C.H. Lam, *IBM J. Res. Dev.* **52**, 465 (2008)
57. I.H. Inoue, S. Yasuda, H. Akinaga, H. Takagi, *Phys. Rev. B* **77**, 035105 (2008)
58. A. Sawa, *Mat. Today* **11**, 28 (2008)
59. S.H. Jo, K.H. Kim, W. Lu, *Nano Lett.* **9**, 870 (2009)
60. S.H. Jo, T. Chang, I. Ebong, B.B. Bhadviya, P. Mazumder, W. Lu, *Nano Lett.* **10**, 1297 (2010)
61. M.J. Lee, C.B. Lee, D. Lee, S.R. Lee, M. Chang, J.H. Hur, Y.B. Kim, C.J. Kim, D.H. Seo, S. Seo, U.I. Chung, I.K. Yoo, K. Kim, *Nature Materials* **10**(8), 625 (2011)
62. A.C. Torrezan, J.P. Strachan, G. Medeiros-Ribeiro, R.S. Williams, *Nanotechnology* **22**(48), 485203 (2011)
63. W.B. Levy, O. Steward, *Neuroscience* **8**, 791 (1983)
64. H. Markram, J. Lubke, M. Frotscher, B. Sakmann, *Science* **275**, 213 (1997)
65. G.Q. Bi, M.M. Poo, *J. Neurosci.* **18**, 10464 (1998)
66. R.C. Froemke, Y. Dan, *Nature* **416**, 433 (2002)
67. Y.V. Pershin, M. Di Ventra, *Proc. IEEE* (in press); arXiv:1009.6025 (2010)
68. G.S. Snider, *SciDAC Review* **10**, 58 (2008)
69. S. Parkin, Innately three dimensional spintronic memory and logic devices: Racetrack memory and spin synapses (2010). Talk at 2010 MRS SprinG Meeting
70. S. Kaeck, G. Banker, *Nat. Protoc.* **1**, 2406 (2006)
71. W.S. Zhao, G. Agnus, V. Derycke, A. Filoramo, J.P. Bourgoin, C. Gamrat, *Nanotechnology* **21**(17), 175202 (2010)
72. Y.V. Pershin, M. Di Ventra, *Phys. Rev. E* **84**, 046703 (2011)
73. K.K. Likharev, D.B. Strukov, in *Introducing Molecular Electronics*, vol. 657, ed. by G.F. G. Cuniberti, K. Richter (Springer, 2005), pp. 447–477